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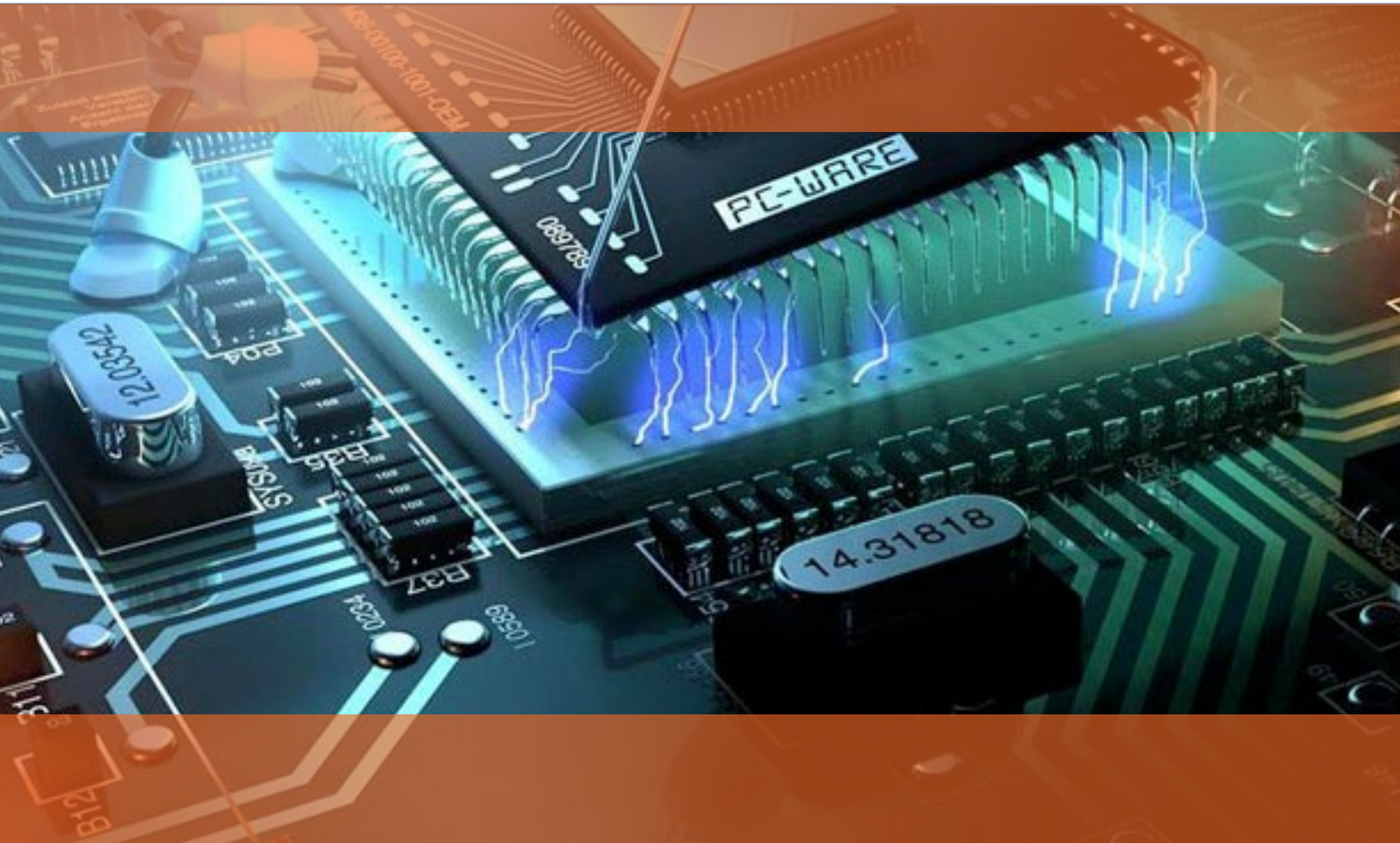
ACCELERATING DESIGN VERIFICATION

Allegro Selects Agnisys IDesignSpec™ and ARV-Sim™ for Specification Creation, Automatic HDL and UVM Model Generation for Register and Memory Blocks



About Allegro MicroSystems LLC:

Allegro develops integrated circuit solutions focused on motor control, regulation, and magnetic field sensing applications. Allegro provides highly integrated mixed-signal ICs, adding more components and greater functionality. Allegro's line has extensive product breadth and depth, with standard "plug and play" products.

- Market leading Hall-effect sensor IC manufacturer with a broad portfolio of innovative solutions focused on the automotive market space
- Customized packaging solutions that incorporate magnetic circuits to simplify applications issues
- System-On-Chip power IC capability incorporating multiple power drivers, regulators, and control logic functions
- Proprietary BCD (Bi-polar, CMOS, DMOS) and BiCMOS wafer process technology that allows the merging of dense digital circuitry with power and or magnetic sensing structures

How Allegro used IDesignSpec and ARV-Sim:

All new Allegro designs use Agnisys IDesignSpec for specification creation, automatic HDL generation and UVM register model generation for the register/memory blocks. This methodology enhancement has already brought much-needed consistency from common template based word document specifications, productivity and efficiency gains during the product development cycle across all projects.

Allegro designs also have had additional challenges that are not uncommon in the industry. For example, features like memory shadowing, aliasing, timers, customer locking and security. These added features required Allegro to spend time in the verification of these blocks since the UVM built-in library tests did not address these additional design features of the register blocks. In addition, it was hard to get adequate test coverage for the hardware updates of the registers in the system level test environment. Allegro's digital designs strictly follow test plan and coverage based - Matrix Driven Verification (MDV) flow. To satisfy MDV flow, besides coding of the test benches, tests and models, the verification team had to write test plans, link them to a proper functional coverage matrix and then generate reports (Matrix report). Agnisys tools addressed these challenges.

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The Benefits Realized by Allegro From Using IDesignSpec and ARV-Sim:

ARV-Sim is a complete register verification solution that integrates with Synopsys VCS®, Cadence Incisive® and Mentor Questa® simulators. Allegro Micro Systems uses ARV-Sim to automatically generate all files required for UVM based verification of registers and memories for their Cadence Incisive based verification environment.

> "We believe that the Agnisys ARV-Sim product provides a complete standalone verification solution for register/memory blocks that is completely turnkey and best of all; it requires no additional effort from the verification team to satisfy the MDV flow requirements,"
>
> Khalid Chishti, Design Verification Manager, Allegro Micro Systems, LLC.

ARV-Sim completely automates the UVM verification process. This approach eliminates the lengthy and error prone UVM test bench and sequence creation process. ARV-Sim provides the positive and negative sequences automatically – the actual test sequences that stimulate the hardware to ensure that the implementation is correct. ARV-Sim not only tests the register implementation but also the interface between the registers and the application logic.

ARV-Sim Ensures the Register Implementation is Correct:

- ARV-Sim ensures that the coverage metrics are achieved. The only way to know you have tested all scenarios is by the coverage. ARV provides the coverage metrics and writes tests to enable 100% coverage on the registers.
- ARV-Sim supports testing of special registers, for example, lock registers, shadow registers, register aliases, interrupts etc. It generates sequences for these special registers.
- ARV-Sim ensures that the application logic correctly interfaces with the registers and memories.
- Automatically creates register-focused coverage reports.
- User can check either the IDesignSpec generated RTL code, the user's own implementation, or a mix of the two with standard buses or user defined buses and transactions.
- Being an add-on to IDesignSpec, users can import IP-XACT, SystemRDL, RALF, Word, Excel, CSV, XML and host of other formats.

Schedule a Live IDesignSpec Demonstration

Schedule a Live ARV Demonstration

Schedule an ARV Evaluation

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